UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,418	10/16/2003	Tsvika Kurts	042390.P15471	7820

45209 7590 11/06/2009
INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
ROJAS, DANIEL E	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
11/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	**Application No.** 10/685,418	**Applicant(s)** KURTS ET AL.	
	Examiner DANIEL ROJAS	**Art Unit** 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 September 2009_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,3-26,34,36,65 and 66_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,3-26,34,36,65 and 66_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 66 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's variable transistor 1118 does not have a second terminal which is only coupled to a source terminal of the switch transistor. When transistor 1116 is on, then the second terminal of the variable transistor will be connected to the drain of 114 and all of the pass gates. Thus, claim 66 is considered misdescriptive. For the purposes of examination, examiner will interpret the limitation of “a second terminal of the variable impedance transistor is coupled to only a source terminal of the switch transistor” as “a second terminal of the variable impedance transistor is coupled to the switch transistor.”

Response to Arguments

3. Applicant's arguments filed 9/28/2009 have been fully considered but they are not persuasive.

4. Applicant’s first argument is as follows:

5. “…the control signal of both pass gates is a same control signal such that the pass gates function as one buffer as intended (Lo, Figure 14). Therefore, Lo also fails to disclose "wherein an impedance of each of said pass gates is to be controlled by a respective control signal.” Lin and Lo, even if combined, would still fail to teach all

the elements of claim 1. Furthermore, Lo discloses using pass gates as a buffer, but fails to teach controlling impedance of each of the pass gates. Thus, one skilled in the art would not look into Lo for controlling impedance of each of pass gates. Therefore, it is not obvious to combine Lin and Lo."

6. It is noted that the previous office action used the Lo reference only to teach the substitution of a pass transistor and a pass gate as art recognized equivalents. The previous office action states on page 2 that "it would have been obvious to one of ordinary skill in the art at the time of invention to replace Lin's transistor (47-53) with pass gates in order to achieve fully rail to rail voltage swings, as taught by Lo (in [0038]). Thus, the use of Lo's pass gates within his circuit relates only to the intended use of said pass gates. As noted in applicant's response, Lin describes that the load can be adjusted through operation of switches 47-54 (column 3, line 67 to column 4, line 17). Thus, when pass gates are used in place of Lin's pass transistors (as taught by Lo), control signals control the on/off operation of each pass gate (i.e. the impedance is controlled).
7. Applicant's second argument is as follows:
8. "Sharp states that "transistor 23 [a]ffects the input to the inverter 24 in the same manner as transistor 16 [a]ffects the buffered reference potential on line 19"...Sharp requires all transistor to be preselected and matched so that the compensation circuit is operable. In short, Sharp does not disclose a variable impedance transistor."

9. For temperature compensation to occur in Sharp's circuit, the change in an operational or reference voltage must be compensated with a change in the impedance of Sharp's transistors. Thus, over a change in temperature, the signal applied to the gate of transistor 23 will change, causing the impedance of transistor 23 to change.

10. Applicant's arguments with respect to claims 11, 17, 65, and 66 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 2, 7-10, 18-21, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent No. 6,868,504) in view of Lo et al (US Patent Application Publication No. 2003/0102894), hereinafter referred to as Lin and Lo, respectively.

13. For claim 1, Lin teaches in his Figure 3 a programmable delay cell comprising a capacitor coupled to a low supply rail (within 63, on the right); a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell (Out); but fails to teach two or more pass gates coupled to said conductor and to said capacitor. However, Lo teaches replacing transistors with pass gates ([0027] and as shown in comparison of Figure 7 with Figure 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to replace Lin's transistors (47-53) with pass gates "in order to achieve fully rail to rail voltage swings," as taught by Lo (in [0038]). Furthermore, the substitution of one known element for another would have yielded predictable results to one having ordinary skill in the art at the time of invention. It is understood to one of ordinary skill in the art that a single transistor that acts as a switch to enable/disable a signal provided at an input node to an output node is considered a pass gate (i.e. two transistors and parallel are not required for a pass gate). Thus, transistors 3 and 4 within Lo's pass gate can each be considered pass gates. Therefore, the combination of Lin and Lo teaches two or more pass gates (3 and 4, Lo) coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor (inherent, based on the structure of the combination, as explained above), wherein an impedance of each of said pass gates is to be controlled by a respective control signal (as explained in Response to Arguments section above).

14. For claim 7, Lin teaches in his Figure 3 an output buffer (45) to generate an electrical signal on a conductor coupled to said controller; and a programmable delay cell comprising a capacitor coupled to a low supply rail (within 63, on the right); a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell; but fails to teach two or more pass gates coupled to

said conductor and to said capacitor. However, Lo teaches replacing transistors with pass gates ([0027] and as shown in comparison of Figure 7 with Figure 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to replace Lin's transistors (47-53) with pass gates "in order to achieve fully rail to rail voltage swings," as taught by Lo (in [0038]). Furthermore, the substitution of one known element for another would have yielded predictable results to one having ordinary skill in the art at the time of invention. It is understood to one of ordinary skill in the art that a single transistor that acts as a switch to enable/disable a signal provided at an input node to an output node is considered a pass gate (i.e. two transistors and parallel are not required for a pass gate). Thus, transistors 3 and 4 within Lo's pass gate can each be considered pass gates. Therefore, the combination of Lin and Lo teaches two or more pass gates (3 and 4, Lo) coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor (inherent, based on the structure of the combination, as explained above) wherein an impedance of each of said pass gates is to be controlled by a respective control signal (as explained in Response to Arguments section above).

15. For claim 8, Lin teaches a register (76, Figure 5) coupled to said programmable delay cell (as explained in column 2, lines 42-43) to store a value that determines a

time delay introduced by said programmable delay cell (inherently, based upon the structure).

16. For claim 9, the combination of Lin and Lo fail to teach a memory device storing values to program a register. Examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.
17. For claim 10, the implementation of the controller defined by claim 7 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 7 as a memory controller relates only to the intended use of claim 7. Furthermore, the combination circuit of Lin and Lo teaches a controller which is capable of being a memory controller.
18. For claim 18, Lin teaches in his Figure 3 a controller comprising an input buffer (44) to receive an electrical signal from a conductor coupled to said controller (inherent based upon the structure); a capacitor coupled to a low supply rail (within 63, on the right); a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell; but fails to teach two or more pass gates coupled to said conductor and to said capacitor. However, Lo teaches replacing transistors with pass gates ([0027] and as shown in comparison of Figure 7 with

Figure 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to replace Lin's transistors (47-53) with pass gates "in order to achieve fully rail to rail voltage swings," as taught by Lo (in [0038]). Furthermore, the substitution of one known element for another would have yielded predictable results to one having ordinary skill in the art at the time of invention. It is understood to one of ordinary skill in the art that a single transistor that acts as a switch to enable/disable a signal provided at an input node to an output node is considered a pass gate (i.e. two transistors and parallel are not required for a pass gate). Thus, transistors 3 and 4 within Lo's pass gate can each be considered pass gates. Therefore, the combination of Lin and Lo teaches two or more pass gates (3 and 4, Lo) coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor (inherent, based on the structure of the combination, as explained above), wherein an impedance of each of said pass gates is to be controlled by a respective control signal (as explained in the Response to Arguments section).

19. For claim 19, Lin teaches a register (76, Figure 5) coupled to said programmable delay cell (as explained in column 2, lines 42-43) to store a value that determines a time delay introduced by said programmable delay cell (inherently, based upon the structure).

20. For claim 20, the combination of Lin and Lo fail to teach a memory device storing values to program a register. Examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

21. For claim 21, the implementation of the controller defined by claim 18 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 18 as a memory controller relates only to the intended use of claim 18. Furthermore, the combination circuit of Lin and Lo teaches a controller which is capable of being a memory controller.

22. For claim 34, examiner takes official notice that many circuits and chips and be implemented on a circuit board and therefore, any circuit is capable of being implemented on the same printed circuit board as a graphics chip. Lin teaches in his Figure 5 a controller comprising the programmable delay cell of Figure 3 wherein Figure 3 comprises a programmable delay cell comprising a capacitor coupled to a low supply rail (within 63, on the right); a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell; but fails to teach two or more pass gates coupled to said conductor and to said capacitor. However, Lo teaches replacing transistors with pass gates ([0027] and as shown in

comparison of Figure 7 with Figure 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to replace Lin's transistors (47-53) with pass gates "in order to achieve fully rail to rail voltage swings," as taught by Lo (in [0038]). Furthermore, the substitution of one known element for another would have yielded predictable results to one having ordinary skill in the art at the time of invention. It is understood to one of ordinary skill in the art that a single transistor that acts as a switch to enable/disable a signal provided at an input node to an output node is considered a pass gate (i.e. two transistors and parallel are not required for a pass gate). Thus, transistors 3 and 4 within Lo's pass gate can each be considered pass gates. Therefore, the combination of Lin and Lo teaches two or more pass gates (3 and 4, Lo) coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor (inherent, based on the structure of the combination, as explained above) wherein the impedance of each of said pass gates is to be controlled by a respective control signal (as explained in the Response to Arguments section above).

23. For claim 65, the combination of Lin and Lo as defined above teaches the use of at least 4 pass gates.

24. Claims 3 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Lo and Sharp (US Patent No. 4,584,492), hereinafter referred to as Lin, Lo, and Sharp, respectively.

25. For claim 3, the combination of Lin and Lo as defined above teaches the limitations of claim 1 but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure 1) comprising a variable impedance transistor (23) coupled to a high supply rail (as shown), wherein an impedance of said variable impedance transistor is to be determined by a control signal (18). Sharp teaches in his specification that “the feedback on line 18 compensates for the temperature changes and process variations” (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of invention to use Sharp’s temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (abstract).

26. For claim 36, the combination of Lin and Lo as defined above teaches the limitations of claim 34 but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure 1) comprising a variable impedance transistor (23) coupled to a high supply rail (as shown), wherein an impedance of said variable impedance transistor is to be determined by a control signal (18). Sharp teaches in his specification that “the feedback on line 18 compensates for the temperature changes and process variations” (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of

invention to use Sharp's temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (abstract).

27. Claims 4-6 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Sharp.

28. For claim 4, Lin teaches (Figure 3) a conductor (wire connected to a node between the input of 45 and 54) coupled to an output of said programmable delay cell (OUT); but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure 1) comprising a switch transistor (20) and a variable impedance transistor (23) coupled to a high supply rail (as shown) and to a source terminal of the switch transistor (as shown and further explained below), wherein an impedance of said variable impedance transistor is to be determined by a control signal (18). Sharp teaches in his specification that "the feedback on line 18 compensates for the temperature changes and process variations" (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of invention to use Sharp's temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (as explained by the abstract). It is noted that the claim does not require that the variable impedance transistor is coupled directly between the high supply rail and the source terminal of the switch transistor, only that it is coupled to both.

29. For claim 5, Sharp teaches that his control signal (18) compensates for variations in temperature (abstract).

30. For claim 6, Sharp further teaches that said control signal is a continuous signal (inherent based upon the structure).

31. For claim 66, Sharp further teaches that a first erminal of the variable impedance transistor is coupled to a high supply rail (as shown) and a second terminal of the variable impedance transistor is coupled to the switch transistor (as shown).

32. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Lo in further view of Ota et al (US Patent No 5,568,068).

33. For claim 11, the combination of Lin and Lo teach the limitations of claim 7 but fail to teach the limitations of claim 11. Ota teaches in his Figure 14 a programmable output buffer comprising one or two registers (within 304, as explained below) coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer (as explained below). Ota teaches that "the control circuit 304 comprises an n bit shift register, which is shifted up by a pulse of signal 216 and is shifted down by a pulse of signal 217. The content of the register is outputted as signals 229. According to a state of n bit signals 229 which is outputted from the control circuit 304, each tri-state buffer TS1-TSn are switched to an active or a disable state. The current which is supplied to the load is increased by increasing the number of tri-state buffers which are turned active." It would have been obvious to one of ordinary skill in the art to use Ota's's programmable output

buffer in place of Lin's output buffer 45 in order to provide a means of regulating driving current. Furthermore, the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

35. Claims 12-16 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Sharp.

36. For claims 12 and 13, Lin teaches in his Figure 3 an output buffer (45) to generate an electrical signal on a conductor coupled to said controller (inherently); and a programmable delay cell coupled to said output buffer, wherein said programmable delay cell includes at least: a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure 1) comprising a switch transistor (20) and a variable impedance transistor (23) coupled to a high supply rail (as shown) and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal (18). Sharp teaches in his specification that "the feedback on line 18 compensates for the temperature changes and process variations" (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of invention to use Sharp's temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (abstract). It is noted that the claim does not require that the variable

impedance transistor is coupled directly between the high supply rail and the source terminal of the switch transistor, only that it is coupled to both.

37. For claim 14, Lin teaches a register (76, Figure 5) coupled to said programmable delay cell (as explained in column 2, lines 42-43) to store a value that determines a time delay introduced by said programmable delay cell (inherently, based upon the structure).

38. For claim 15, the combination of Lin and Sharp fails to teach a memory device storing values to program a register. Examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

39. For claim 16, the implementation of the controller defined by claim 12 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 12 as a memory controller relates only to the intended use of claim 12. Furthermore, the combination circuit of Lin and Sharp teaches a controller which is capable of being a memory controller.

40. For claims 22 and 23, Lin teaches a controller (Figure 5) comprising: an input buffer (44, Figure 3) to receive an electrical signal from a conductor coupled to said controller; and a programmable delay cell coupled to said output buffer, wherein said

programmable delay cell includes at least: a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure 1) comprising a switch transistor (20) and a variable impedance transistor (23) coupled to a high supply rail (as shown) and to a source terminal of the switch transistor (as explained below), wherein an impedance of said variable impedance transistor is to be determined by a control signal (18). Sharp teaches in his specification that “the feedback on line 18 compensates for the temperature changes and process variations” (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of invention to use Sharp’s temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (abstract). It is noted that the claim does not require that the variable impedance transistor is coupled directly between the high supply rail and the source terminal of the switch transistor, only that it is coupled to both.

41. For claim 24, Lin teaches a register (76, Figure 5) coupled to said programmable delay cell (as explained in column 2, lines 42-43) to store a value that determines a time delay introduced by said programmable delay cell (inherently, based upon the structure).

42. For claim 25, the combination of Lin and Sharp fails to teach a memory device storing values to program a register. Examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive

data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

43. For claim 26, the implementation of the controller defined by claim 12 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 12 as a memory controller relates only to the intended use of claim 12. Furthermore, the combination circuit of Lin and Sharp teaches a controller which is capable of being a memory controller.

44. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Sharp in view of Ota.

45. For claim 17, the combination of Lin and Sharp as defined above teaches the limitations of claim 12 but fails to teach the limitations of claim 17. Ota teaches in his Figure 14 a programmable output buffer comprising one or two registers (within 304, as explained below) coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer (as explained below). Ota teaches that “the control circuit 304 comprises an n bit shift register, which is shifted up by a pulse of signal 216 and is shifted down by a pulse of signal 217. The content of the register is outputted as signals 229. According to a state of n bit signals 229 which is outputted from the control circuit 304, each tri-state buffer TS1-TSn are switched to

an active or a disable state. The current which is supplied to the load is increased by increasing the number of tri-state buffers which are turned active." It would have been obvious to one of ordinary skill in the art to use Ota's programmable output buffer in place of Lin's output buffer 45 in order to provide a means of regulating driving current. Furthermore, the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. R./
Examiner, Art Unit 2816
/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816